74HC4040; 74HCT4040

12-stage binary ripple counter

Rev. 03 — 14 September 2005 Product data sheet

1. General description

The 74HC4040; 74HCT4040 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4040B series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4040; 74HCT4040 are 12-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

2. Features

- Multiple package options
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC4040						
t_{PHL}, t_{PLH}	propagation delay					
	$\overline{CP}$ to Q0	C_L = 15 pF; V_{CC} = 5 V	-	14	-	ns
	Qn to Qn+1	C_L = 15 pF; V_{CC} = 5 V	-	8	-	ns

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum operating frequency	C_L = 15 pF; V_{CC} = 5 V	-	90	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	-	20	-	pF
Type 74HCT4040						
t_{PHL}, t_{PLH}	propagation delay					
	$\overline{CP}$ to Q0	C_L = 15 pF; V_{CC} = 5 V	-	16	-	ns
	Qn to Qn+1	C_L = 15 pF; V_{CC} = 5 V	-	8	-	ns
f_{max}	maximum operating frequency	C_L = 15 pF; V_{CC} = 5 V	-	79	-	MHz
C_i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V	-	20	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC4040D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4040DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4040PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4040BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4040N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HCT4040D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

Table 2: Ordering information *…continued*

Type number	Package			
	Temperature range	Name	Description	Version
74HCT4040DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4040PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4040BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

6. Functional diagram

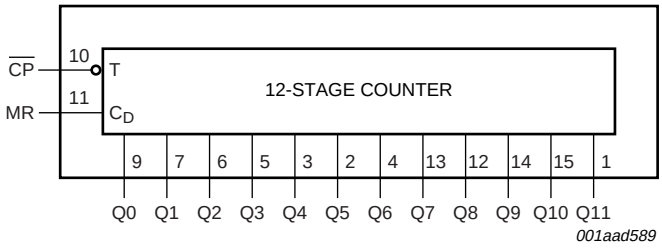


Fig 1. Functional diagram

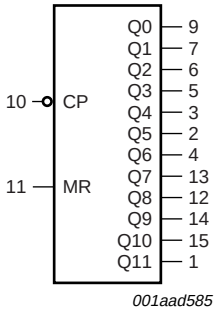


Fig 2. Logic symbol

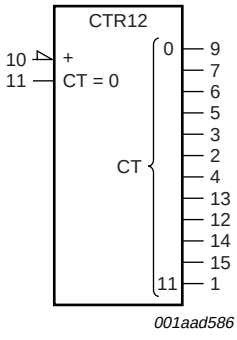


Fig 3. IEC logic symbol

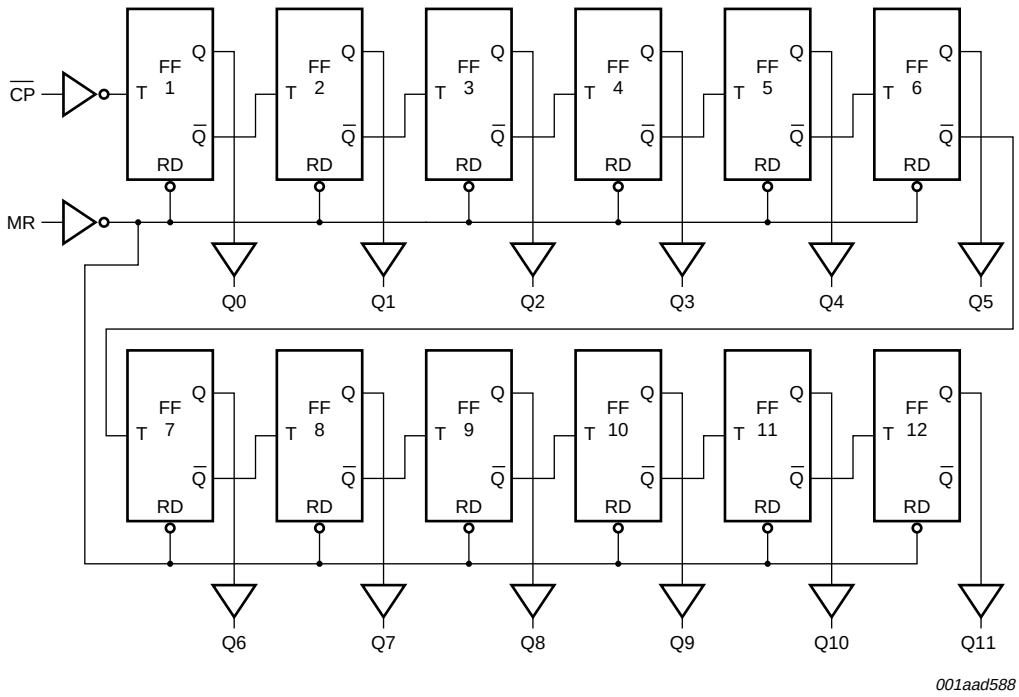


Fig 4. Logic diagram

7. Pinning information

7.1 Pinning

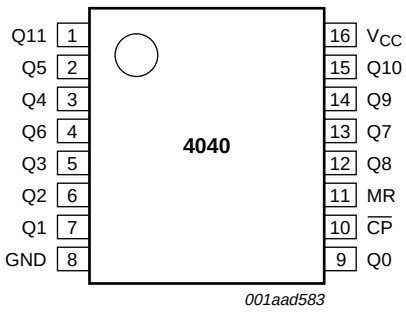
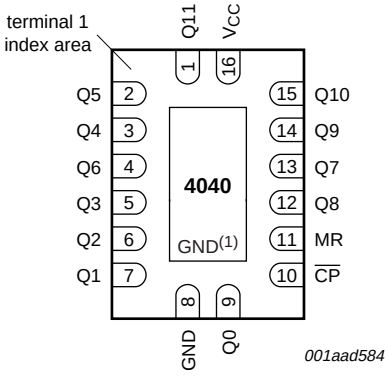


Fig 5. Pin configuration DIP16, SO16, SSOP16 and TSSOP16



Transparent top view

(1) The substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input

Fig 6. Pin configuration DHVQFN16

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
Q11	1	output 11
Q5	2	output 5
Q4	3	output 4
Q6	4	output 6
Q3	5	output 3
Q2	6	output 2
Q1	7	output 1
GND	8	ground (0 V)
Q0	9	output 0
$\overline{CP}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	output 8
Q7	13	output 7
Q9	14	output 9
Q10	15	output 10
V_{CC}	16	positive supply voltage

8. Functional description

8.1 Function table

Table 4: Function table

Input		Output
$\overline{CP}$	MR	Q0 to Q11
↑	L	no change
↓	L	count
X	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW clock transition.

8.2 Timing diagram

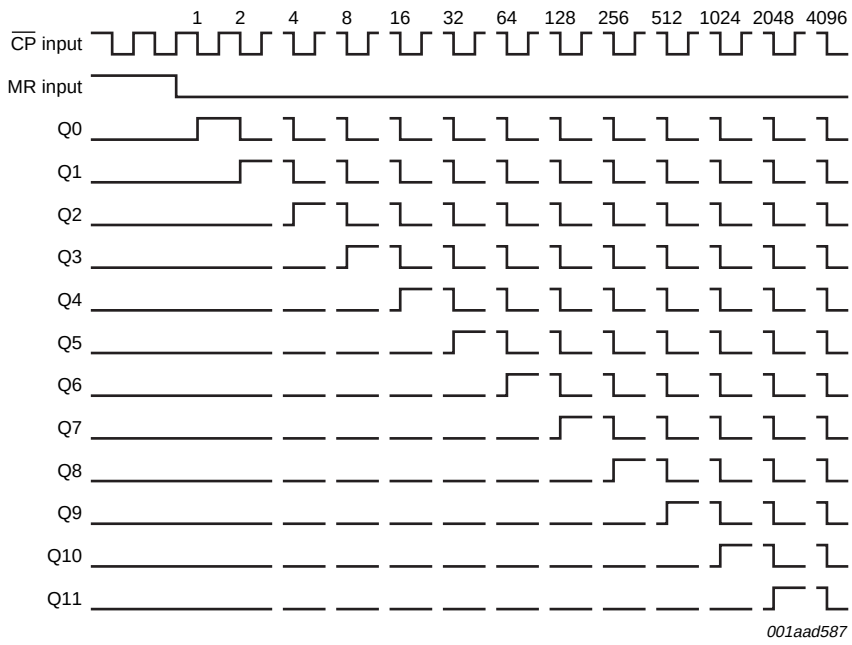


Fig 7. Timing diagram

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_O	output source or sink current	$–0.5$ V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	quiescent supply current			-	±50	mA
I_{GND}	ground current			-	±50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[1]			
	DIP16 package			-	750	mW
	SO16, SSOP16, TSSOP16 and DHVQFN16 packages			-	500	mW

[1] For DIP16 packages: above 70 °C, P_{tot} derates linearly with 12 mW/K.
For SO16, SSOP16, TSSOP16 and DHVQFN16 packages, above 70 °C, P_{tot} derates linearly with 8 mW/K.

10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
type 74HC4040						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	see Section 11 and 12 per device	–40	-	+125	°C
t_r, t_f	input rise and fall times	except for Schmitt-trigger inputs				
		V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
type 74HCT4040						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	see Section 11 and 12 per device	–40	-	+125	°C
t_r, t_f	input rise and fall times	except for Schmitt-trigger inputs				
		V_{CC} = 2.0 V	-	-	-	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	-	ns

11. Static characteristics

Table 7: Static characteristics for 74HC4040

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V

Table 7: Static characteristics for 74HC4040 *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V;	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80.0	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V

Table 7: Static characteristics for 74HC4040 *...continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -20$ µA; $V_{CC} = 6.0$ V	5.9	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
		$I_O = -5.2$ mA; $V_{CC} = 6.0$ V;	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 20$ µA; $V_{CC} = 6.0$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
		$I_O = 5.2$ mA; $V_{CC} = 6.0$ V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	160.0	µA

Table 8: Static characteristics for 74HCT4040

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	0	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		$\overline{CP}$	-	85	306	µA
		MR	-	110	396	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V

Table 8: Static characteristics for 74HCT4040 *…continued*

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.84	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80.0	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		$\overline{CP}$	-	-	383	µA
		MR	-	-	495	µA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 4.5$ V	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 4.0$ mA; $V_{CC} = 4.5$ V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	160.0	µA
ΔI_{CC}	additional quiescent supply current	$V_I = V_{CC} - 2.1$ V; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A				
		$\overline{CP}$	-	-	417	µA
		MR	-	-	539	µA

12. Dynamic characteristics

Table 9: Dynamic characteristics for type 74HC4040

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	47	150	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	17	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	14	26	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	28	100	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	10	20	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	8	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	8	17	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} =2.0 V; C_L = 50 pF	-	61	185	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	22	37	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	18	31	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	19	75	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	7	15	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	6	13	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	80	14	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	16	5	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	14	4	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	80	22	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	16	8	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	14	6	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	50	8	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	10	3	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	9	2	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	6.0	27	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	30	82	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	90	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	35	98	-	MHz
C_{PD}	power dissipation capacitance		-	20	-	pF

Table 9: Dynamic characteristics for type 74HC4040 *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	190	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	38	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	33	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	125	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	25	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	21	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	230	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	46	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	39	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	95	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	19	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	16	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	100	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	17	-	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	100	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	17	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	65	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	13	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	11	-	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	4.8	-	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	28	-	-	MHz

Table 9: Dynamic characteristics for type 74HC4040 *…continued*

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	225	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	45	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	38	ns
	propagation delay Qn to Qn+1	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	150	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	30	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	26	ns
t_{PHL}	propagation delay MR to Qn	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	280	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	56	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	-	-	110	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	-	22	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	-	19	ns
t_W	clock pulse width HIGH or LOW	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	120	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	20	-	-	ns
	master reset pulse width; HIGH	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	120	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	24	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	20	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	75	-	-	ns
		V_{CC} = 4.5 V; C_L = 50 pF	15	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	13	-	-	ns
f_{max}	maximum operating frequency	see Figure 8				
		V_{CC} = 2.0 V; C_L = 50 pF	4.0	-	-	MHz
		V_{CC} = 4.5 V; C_L = 50 pF	20	-	-	MHz
		V_{CC} = 6.0 V; C_L = 50 pF	24	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

Table 10: Dynamic characteristics for type 74HCT4040

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	see Figure 8					
		V_{CC} = 4.5 V; C_L = 50 pF		-	19	40	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	16	-	ns
	propagation delay Qn to Qn+1	see Figure 8					
		V_{CC} = 4.5 V; C_L = 50 pF		-	10	20	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	8	-	ns
t_{PHL}	propagation delay MR to Qn	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	23	45	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	7	15	ns
t_W	clock pulse width HIGH or LOW	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		16	7	-	ns
	master reset pulse width; HIGH	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		16	6	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		10	2	-	ns
f_{max}	maximum operating frequency	see Figure 8					
		V_{CC} = 4.5 V; C_L = 50 pF		30	72	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	79	-	MHz
C_{PD}	power dissipation capacitance per package		[1]	-	20	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	-	50	ns
	propagation delay Qn to Qn+1	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	-	25	ns
t_{PHL}	propagation delay MR to Qn	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	-	56	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	-	19	ns
t_W	clock pulse width HIGH or LOW	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		20	-	-	ns
	master reset pulse width; HIGH	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		20	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		13	-	-	ns
f_{max}	maximum operating frequency	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		24	-	-	MHz
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay $\overline{CP}$ to Q0	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8;		-	-	60	ns
	propagation delay Qn to Qn+1	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8		-	-	30	ns

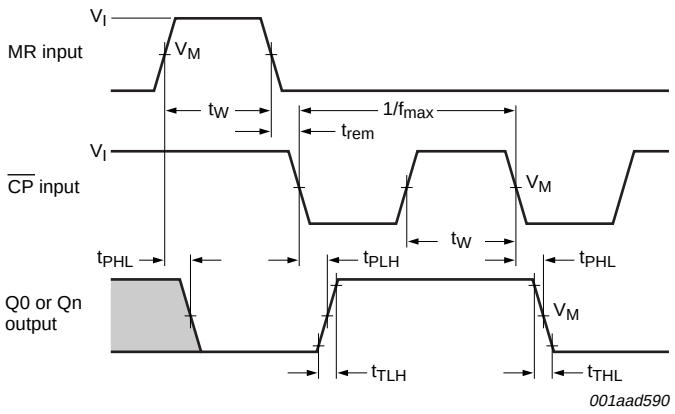
Table 10: Dynamic characteristics for type 74HCT4040 *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns. For test circuit see Figure 9.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}	propagation delay MR to Qn	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	-	-	68	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	-	-	22	ns
t_W	clock pulse width HIGH or LOW	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	24	-	-	ns
	master reset pulse width; HIGH	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	24	-	-	ns
t_{rec}	recovery time MR to $\overline{CP}$	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	15	-	-	ns
f_{max}	maximum operating frequency	V_{CC} = 4.5 V; C_L = 50 pF; see Figure 8	20	-	-	MHz

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

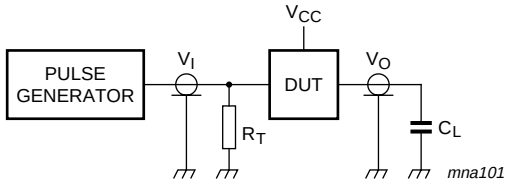
13. Waveforms



74HC4040: V_M = 50 %; V_I = GND to V_{CC}.

74HCT4040: V_M = 1.3 V; V_I = GND to 3 V.

Fig 8. Clock ($\overline{CP}$) to output (Qn) propagation delays, clock pulse width, output transition times, maximum clock pulse frequency, master reset (MR) pulse width, master reset to output (Qn) propagation delays and master reset to clock ($\overline{CP}$) removal time.



Definitions for test circuit:

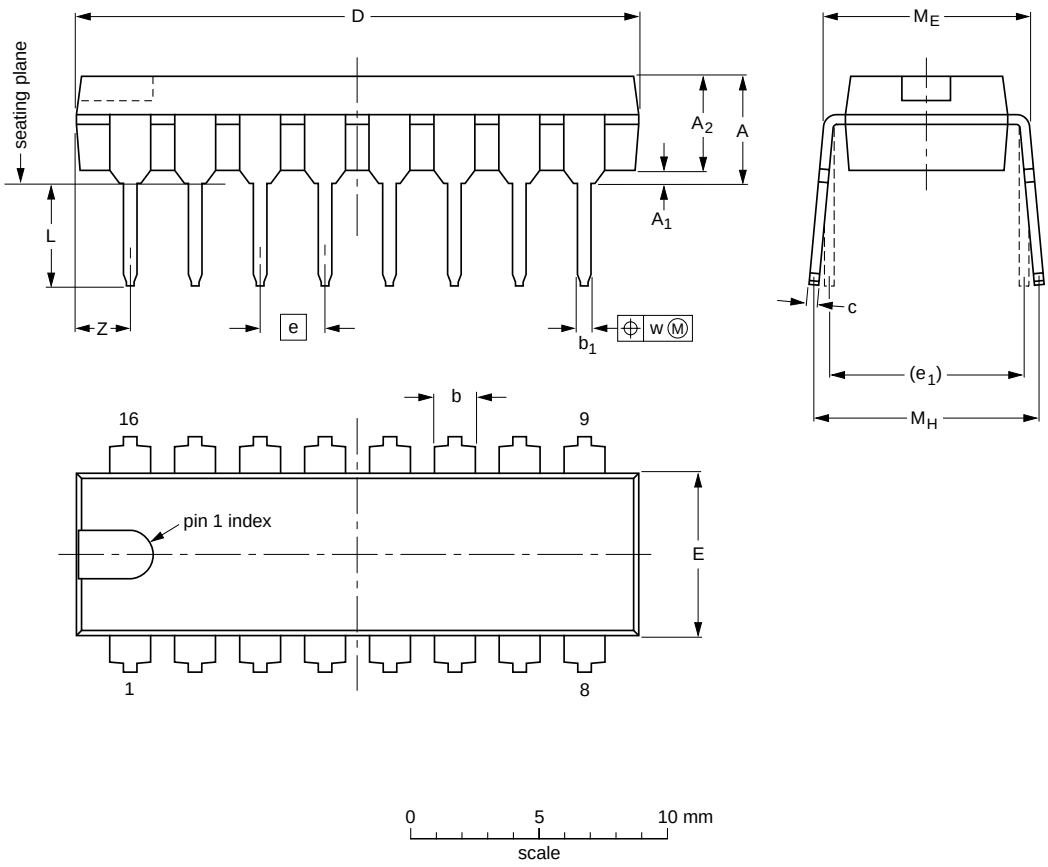
C_L = load capacitance including jig and probe capacitance (See Section 12 for the value).

R_T = termination resistance should be equal to output impedance Z_O of the pulse generator.

Fig 9. Test circuit

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

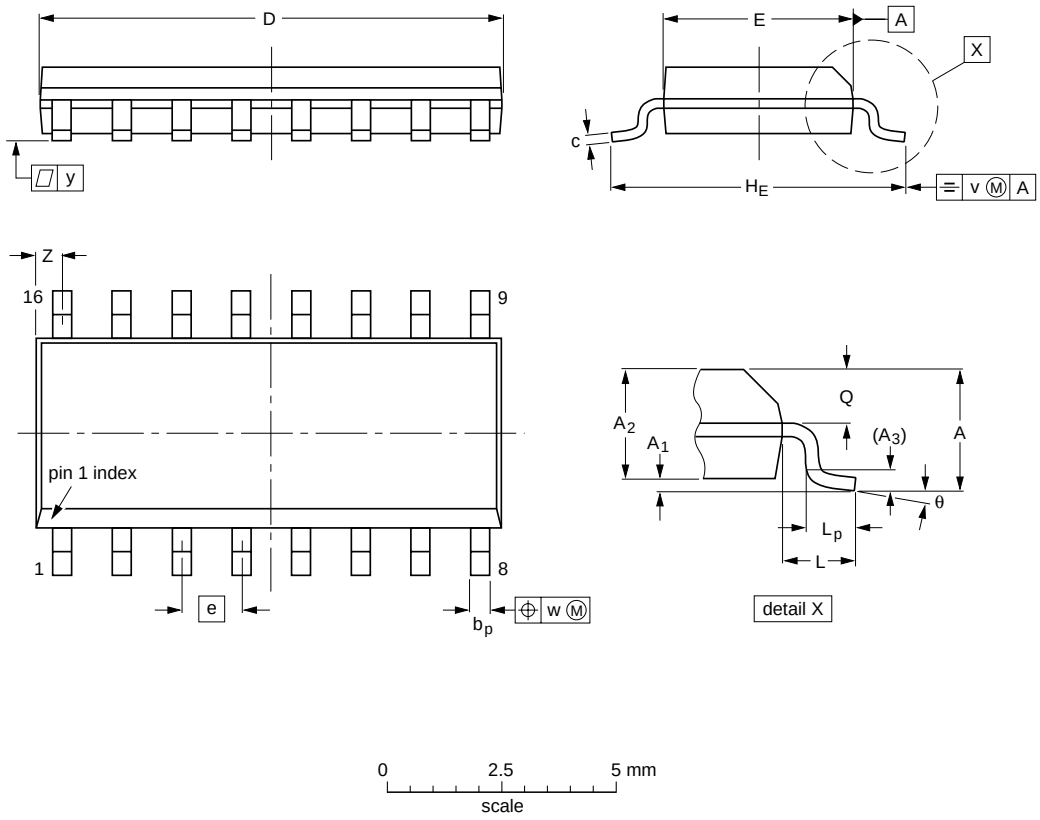
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT38-1 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

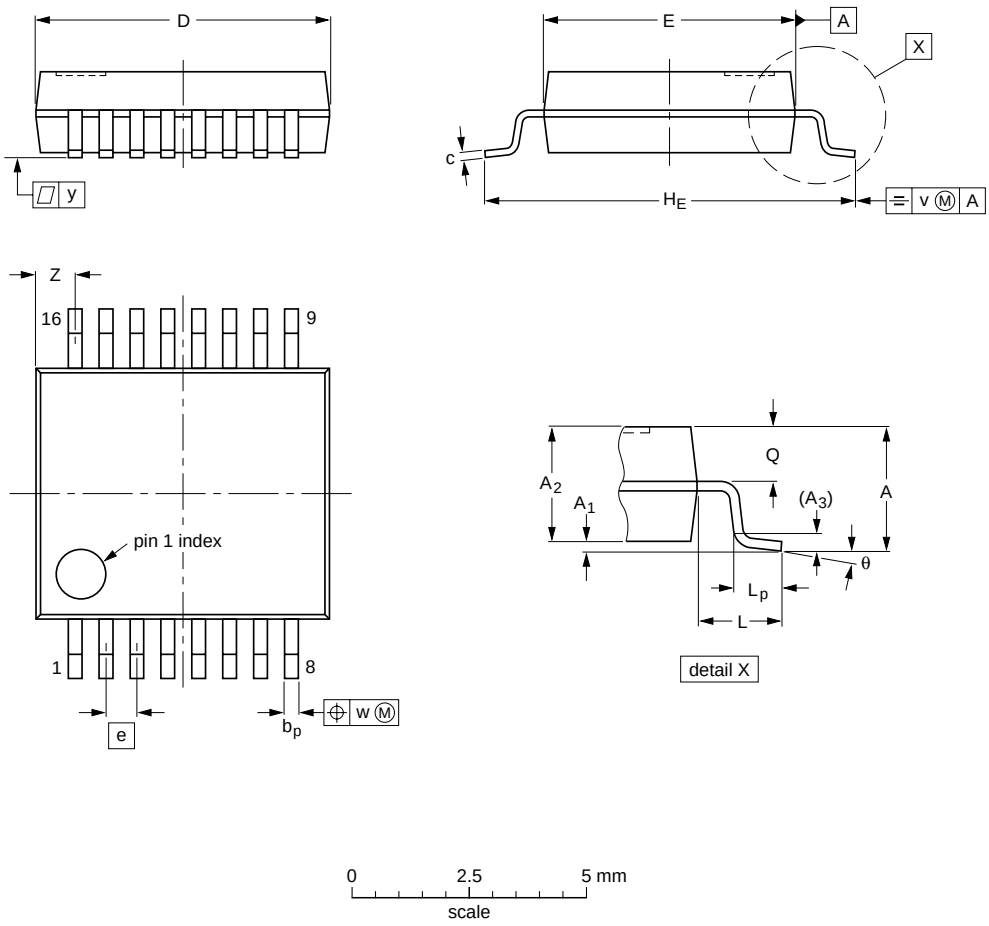
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

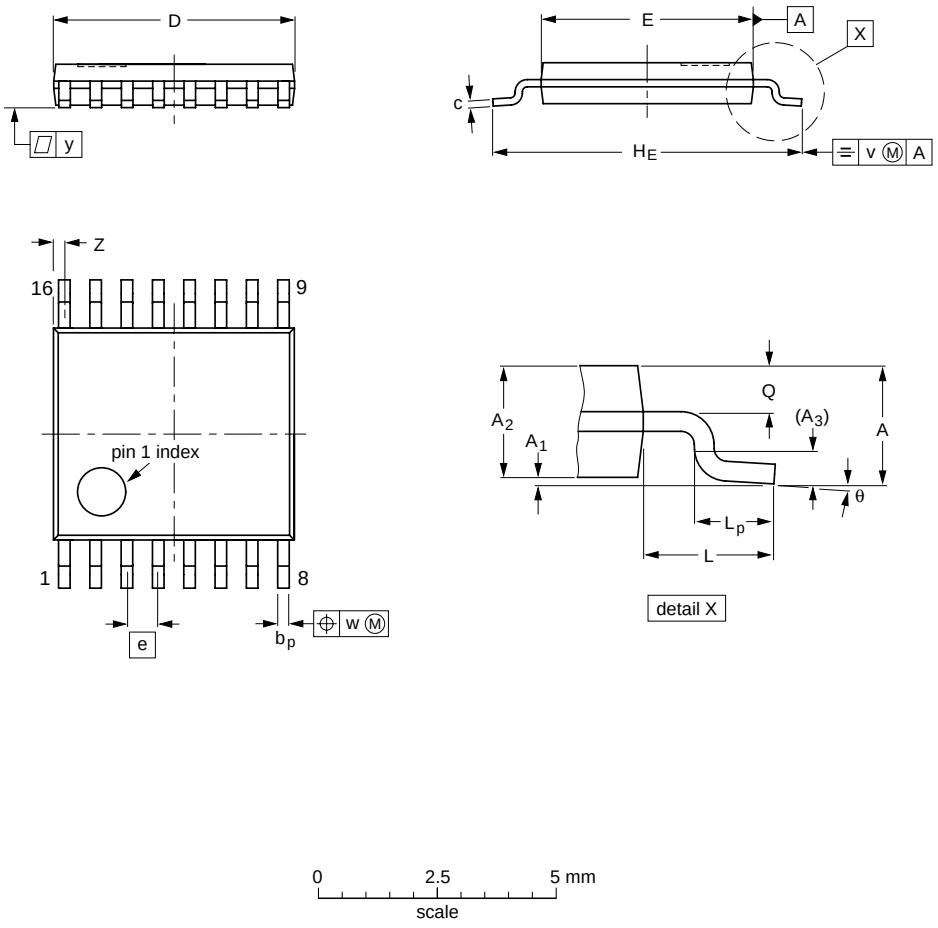
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

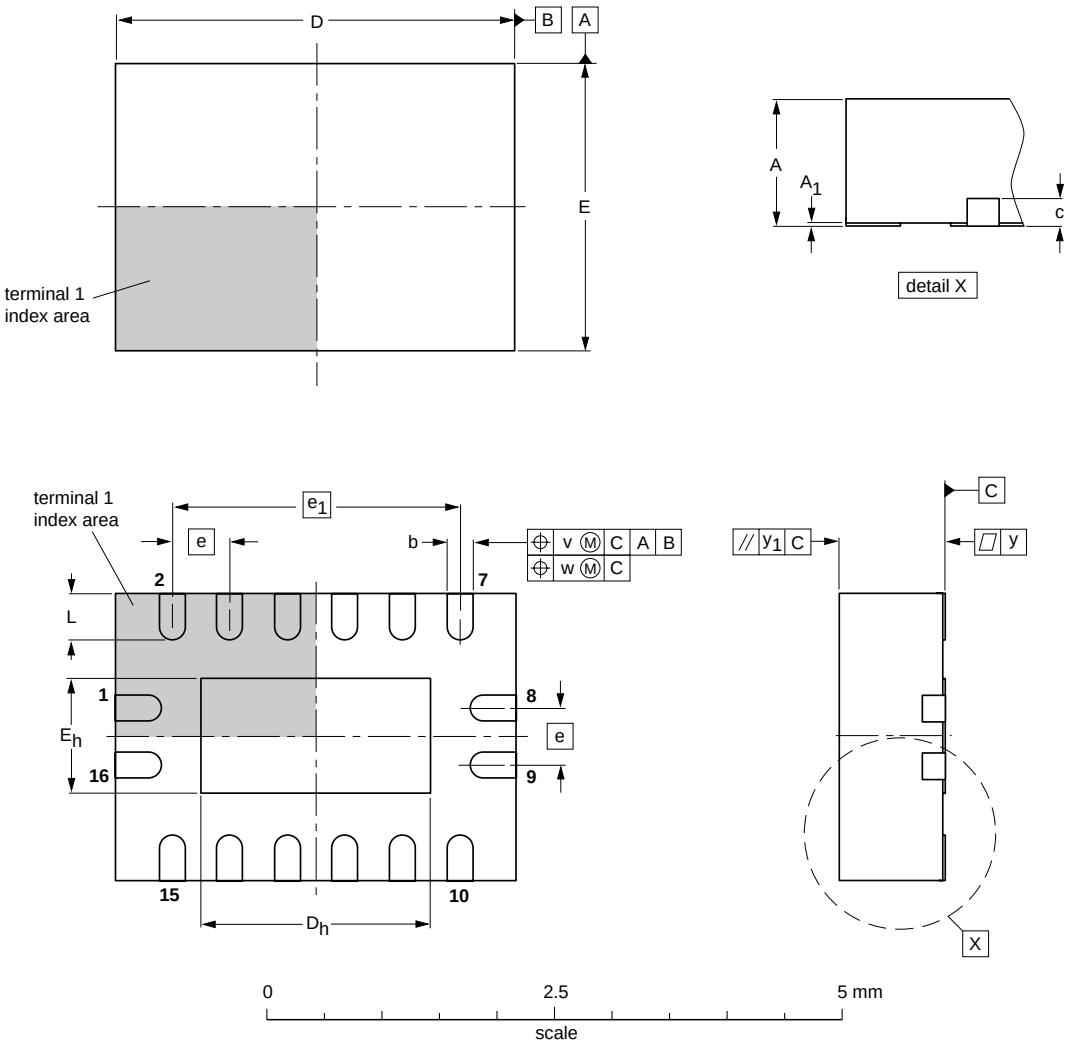
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 14. Package outline SOT763-1 (DHVQFN16)

15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT4040_3	20050914	Product data sheet	-	-	74HC_HCT4040_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Reference to family specifications is replaced by the actual information: Section 5 “Ordering information”, Section 7 “Pinning information”, Section 9 “Limiting values”, Section 10 “Recommended operating conditions”, Section 11 “Static characteristics”, Figure 9 “Test circuit” • Section 14 “Package outline” (DHVQFN16) added				
74HC_HCT4040_CNV_2	19901231	Product specification	-	-	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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